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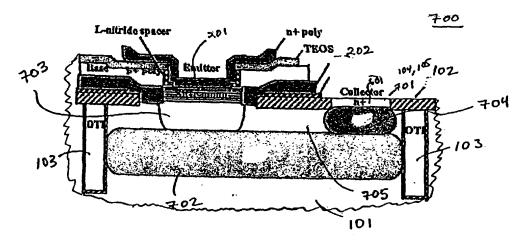
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(54) Title: METHOD OF FABRICATING A SIGE SEMICONDUCTOR STRUCTURE



(57) Abstract: A method of fabricating an integrated circuit includes providing a substrate and creating base-windows in a layer. The method also includes forming a monocrystalline SiGe base layer in each of the base layers, and polycrystalline SiGe elsewhere. Additionally, the method also includes forming a monocrystalline silicon layer over selectively exposed portions of the surface of the substrate. The integrated circuit beneficially includes silicon-based elements such as a lateral pnp transistor, a varactor, and a polysilicon transistor, which are formed on a common substrate with an npn SiGe bipolar transistor.

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TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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